PSE Conformance Test (ver 4.x) 802.3at PICS Coverage

802.3at PSE PIC's

Sifos® Technologies

ITEM	TEST CASE	SECTION REFERENCE IN IEEE 802.3at	PICS Performa Acceptance Criteria	Value/Comment	Sifos PSA-3000 (PSA Ver 4.x) PSE Conformance Test Suite
PSE1	PSE location	33.2.1	Requirement Spec	Midspan or End point PSE	Conformance Test Declaration
PSE2	Alternative B	33.2.1	SIFOS PSA		Implicitly covered by ALT and POLARITY switching in PSA-3000
PSE3	Alternative A and	33.2.1	SIFOS PSA		
PSE4	PSE behavior	33.2.4.1	SIFOS PSA	Covered in PSE5, PSE7, PSE8, PSE9	
PSE5	Backoff Voltage	33.2.4.1	SIFOS PSA	Backoff voltage between ALT B detections must be < 2.8VDC	Test: det_v **Vbk_off**
PSE6	PSE variable definitions permutations	33.2.4.4	SIFOS PSA	PSE must conform to Type-1 or Type-2 Classification Methods	Test: class_time **Event_Count_1**, **Event_Count_2**, class_lldp **PSE_LLDP_Type_2**
PSE7	Type-2 PSE Mutual Identification	33.2.4.6	SIFOS PSA	When powering a Type 2 PD, assigns a value of '2' to parameter_type if mutual identification is complete	Test: class_time **Event_Count_2**, class_lldp **PSE_LLDP_Type_2**
PSE8	Type-2 PSE Powering Type-1 PD	33.2.4.6	SIFOS PSA	Meets at least the PI Electrical Requirements of Type-1 PSE with option to meet Type-2 Requirements for Icon, Ilim, Tlim, and Ptype	Test: pwrup_pwrcap **Pcon_c0, Icon_%_c0, Icon_%_c1, Icon_%_c2, Icon_%_c3**
PSE9	Applying power	33.2.5	SIFOS PSA	Not until a PD requesting power has been successfully detected	Test: det_range **Rgood_Min, Rgood_Max, Rmid_det, Cgood_Max** (et. al.)
PSE10	Power pairs	33.2.5	SIFOS PSA	Power must be supplied on the same pairs as those used for detection.	Test: det_range **Rgood_Min, Rgood_Max, Rmid_det, Cgood_Max** (et. al.)
PSE11	Detecting PDs	33.2.5.1	SIFOS PSA	Performed via the PSE PI	Test: det_v **Voc**, **Vvalid(Max)**, **Vvalid(Min)** (et. al.)
PSE12	PSE Presents a Non-Valid Signature	33.2.5.1	SIFOS PSA	As defined in Table 33-15	Test: det_rsource **Zout**, pwrdn_time **Rp**
PSE13	Open Circuit Voltage and Short Circuit Current	33.2.5.1	SIFOS PSA	Meet specifications for Voc and Isc in Table 33–4	Test: det_v **Voc**, det_i, **Isc**
PSE14	Backdriven current	33.2.5.1		Not be damaged by up to 5 mA over the range of VPort_PSE	*Not Tested*
PSE15	Output capacitance	33.2.5.1	SIFOS PSA	Cout in Table 33–11	Test: pwrdn_time **Cout**
PSE16	Detection Voltage with a valid PD signature connected	33.2.5.2	SIFOS PSA	Meets Vvalid in Table 33–4	Test: det_v **Vvalid(Max)**, **Vvalid(Min)**
PSE17	Detection Voltage Measurements	3.2.5.2	SIFOS PSA	At least two that create at least ΔVtest difference	Test: det_v **Vvalid(Max)**, **Vvalid(Min)**, **ΔVtest**, **Good_Sig_Det_Pulse**
PSE18	Control slew rate when switching detection voltages	33.2.5.2	SIFOS PSA	Less than Vslew in Table 33–4	Test: det_v **Detection_Slew**
PSE19	Accept as a valid signature	33.2.5.3	SIFOS PSA	Rgood and Cgood, with up to Vos max and Ios max as defined in Table 33–5	Test: det_range **Rgood_Min, Rgood_Max, Rmid_det, Cgood_Max**
PSE20	Reject as an invalid signature	33.2.5.3	SIFOS PSA	Resistance less than Rbad min,resistance greater than Rbad max,or capacitance greater than Cbad min	Test: det_range **Rgood_Min, Rgood_Max, Rmid_det, Cgood_Max**
PSE21	Classification permutations	3.2.6	SIFOS PSA	Meet one allowable permutation in Table 33–8	Test: class_time **Event_Count_1**, **Event_Count_2** class_lldp **PSE_LLDP_Type_1**, **PSE_LLDP_Type_2**
PSE22	Type 1 PSE does not implement Physical Layer classification	3.2.6	SIFOS PSA	Assign all PDs to Class 0	Test: pwrup_pwrcap **Pcon_c0, Icon_%_c0**
PSE23	Type 1 PSE failure to complete classification	3.2.6	SIFOS PSA	Return to IDLE state or assign PD to Class 0	Test: class_err **Vport_CL_err_1**
PSE24	Type 2 PSE failure to complete classification	3.2.6	SIFOS PSA	Return to IDLE state	Test: class_err **Vport_CL_err_1**
PSE25	Provide VClass for 1-Event Physical Layer classification	33.2.6.1	SIFOS PSA	Limited to IClass_LIM as defined by Table 33–10	Test: class_i **Max_Iclass**
PSE26	Classification polarity for 1-Event Physical Layer classification	33.2.6.1	SIFOS PSA	Same as VPort	Test: class_v **Vclass_max, Vclass_min**
PSE27	Classification timing for 1-Event Physical Layer classification	33.2.6.1	SIFOS PSA	In accordance with Tpdc in Table 33–10	Test: class_time **Tpdc**
PSE28	Measurement result of 1-Event Physical Layer classification IClass	33.2.6.1	SIFOS PSA	Classify PD according to observed current based on Table 33–9. **Note**: *Only relevant to PSE's that use classification information for power management purposes.*	Test: pwrup_pwrcap **Pcon_c0**, **Pcon_c1**, **Pcon_c2**, **Pcon_c3**, **Pcon_c4**
PSE29	Measurement timing of 1-Event Physical Layer classification IClass	33.2.6.1	SIFOS PSA	Measurement taken after the minimum relevant class event timing in Table 33–10. **Note**:*Only relevant to PSE's that use classification information for power management purposes.*	Test: pwrup_pwrcap **Pcon_c2**
PSE30	Class 4 result for 1-Event Physical Layer classification with a Type 1 PSE	33.2.6.1	SIFOS PSA	Assign the PD to Class 0	Test: pwrup_pwrcap **Pcon_c4, Icon_%_c4**
PSE31	Type 1 PSE 1-Event Physical Layer classification if IClass is in the range of IClass_LIM	33.2.6.1	SIFOS PSA	Return to IDLE state or assign PD to Class 0	Test: class_err **Vport_CL_lim**
PSE32	Type 2 PSE 1-Event Physical Layer classification if IClass is in the range of IClass_LIM	33.2.6.1	SIFOS PSA	Return to IDLE state	Test: class_err **Vport_CL_err_2**
PSE33	In the CLASS_EV1 and CLASS_EV2 states, provide VClass	33.2.6.2	SIFOS PSA	As defined in Table 33–10	Test: class_v **Vclass_max, Vclass_min**
PSE34	Classification timing in CLASS_EV1 state	33.2.6.2	SIFOS PSA	In accordance with TCLE1 in Table 33–10	Test: class_time **Tcle1**
PSE35	In the CLASS_EV1 and CLASS_EV2 states, measurement result IClass	33.2.6.2	SIFOS PSA	Classify PD according to Table 33–9. **Note**: *Only relevant to PSE's that use classification information for power management purposes.*	Test: pwrup_pwrcap **Pcon_c0**, **Pcon_c1**, **Pcon_c2**, **Pcon_c3**, **Pcon_c4**
PSE36	In the MARK_EV1 and MARK_EV2 states, provide VMark	33.2.6.2	SIFOS PSA	In accordance with Table 33–10	Test: class_v **Vmark**
PSE37	Classification timing in MARK_EV1	33.2.6.2	SIFOS PSA	In accordance with TME1 in Table 33–10	Test: class_time **Tme1**
PSE38	Classification timing in CLASS_EV2 state	33.2.6.2	SIFOS PSA	In accordance with TCLE2 in Table 33–10	Test: class_time **Tcle2**
PSE39	Classification timing in MARK_EV2 state	33.2.6.2	SIFOS PSA	In accordance with TME2 in Table 33–10	Test: class_time **Tme2**
PSE40	Type 2 PSE 2-Event Physical Layer classification if IClass is greater than or equal to IClass_LIM min	33.2.6.2	SIFOS PSA	Returns to IDLE state	Test: class_err **Vport_CL_lim**
PSE41	Current limitation during class events	33.2.6.2	SIFOS PSA	Meet IClass_LIM	Test: class_err **Class_lim**
PSE42	Current limitation during mark events	33.2.6.2	SIFOS PSA	Meet IMark_LIM	Test: class_err **Mark_lim**
PSE43	Measurement timing of 2-Event Physical Layer classification IClass	33.2.6.2	SIFOS PSA	Taken after the minimum relevant class event timing in Table. **Note**: *Only relevant to PSE's that use classification information for power management purposes.*	Test: pwrup_pwrcap **Pcon_c2**, **Icon_%_c4**
PSE44	Class event and mark event voltages polarity	33.2.6.2	SIFOS PSA	Same as VPort	Test: class_v **Vclass_max, Vclass_min**, **Vmark**
PSE45	Voltage level at PI when transition to POWER_ON state	33.2.6.2	SIFOS PSA	Completes 2-Event classification and transitions to POWER_ON with PI voltage greater than or equal to VMark min	Test: class_v **Vmark_min**

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PSE46	Return to IDLE state	33.2.6.2	SIFOS PSA	Maintains PI voltage at VReset for at least TReset min before starting new detection cycle	Test: class_err **Treset**
PSE47	Power supply output	33.2.7	SIFOS PSA	When the PSE provides power to the PI, conforms with Table 33–11	Many Tests: pwrup_xxxx, mps_xxxx, pwrdn_xxxx
PSE48	Load regulation	33.2.7.1	SIFOS PSA	Met with (IHold max × VPort_PSE min) to PType min load step at a rate of change of at least 15 mA/µs max	Test: pwrup_v **Vtrans_min_1**, **Vtrans_max_1**, **Vtrans_min_2**, **Vtrans_max_2**
PSE49	Voltage transients	33.2.7.1		Limited to 3.5 V/µs max for load changes up to 35 mA/µs. **Note**: *This is only relevant and measurable in PSE's where changes in load produce significant changes in voltage .*	*Not Tested*
PSE50	Voltage transients (30 µs to250 µs)	33.2.7.2	SIFOS PSA	No less than KTran_lo below VPort_PSE min and meet requirements of 33.2.7.7.	Test: pwrup_maxi **Ktran_lo**
PSE51	Voltage transients (greater than 250 µs)	33.2.7.2	SIFOS PSA	Meet VPort_PSE specification	Test: pwrup_overId **Vport_lpeak_1**, **Vport_lpeak_2**
PSE52	Power feeding ripple and noise	33.2.7.3	SIFOS PSA	Met for common-mode and/or pair-to-pair noise values for power outputs from (IHold max × VPort_PSE min) to PType min at static operating VPort_PSE	Test: pwrup_v **Vpp_ripple_1**, **Vpp_ripple_2**, **Vpp_noise_1**, **Vpp_noise_2**
PSE53	AC current waveform parameters	33.2.7.4	SIFOS PSA	IPeak minimum equals Equation (33–4) for TCUT minimum and 5% duty cycle minimum.	Test: pwrup_overId **%Ipeak_1**, **%Ipeak_2**
PSE54	Inrush current limit	33.2.7.5	SIFOS PSA	PSE limits the maximum current sourced at the PI	Test: pwrup_inrush **Init_Inrush**, **Max_Inrush_c0**, **Max_Inrush_c4**, **Min_Inrush**, **Tinrush**
PSE55	Inrush current template	33.2.7.5	SIFOS PSA	Current sourced does not exceed the PSE inrush template in Figure 33–14	Test: pwrup_inrush **Init_Inrush**, **Max_Inrush_c0**, **Max_Inrush_c4**
PSE56	Short circuit condition	33.2.7.7	SIFOS PSA	Remove power from PI before IPSEUT is exceeded. Equation (33–6) and Figure 33–15.	Test: pwrup_maxi **Ilim_Peak**, **Ilim_Max_1**, **Ilim_Max_2**
PSE57	Short circuit current and time	33.2.7.7	SIFOS PSA	In accordance with ILIM and TLIM in Table 33–1. **Note**: ***Ilim*** *and* ***Tlim*** *within Table 33-11 do not have upper limits, and since port voltage is allowed to drop below* ***Vport_pse_min*** *per 33.2.7.7, there is effectively no lower limit to* ***Tlim*** *since PSE's may remove power with low voltage at any time according to 3.2.7.1.*	Test: pwrup_maxi **Ilim_Min_1**, **Ilim_Min_2**, **Tlim_1, Tlim_2** **Note**: ***Ilim_Min_1*** *and* ***Ilim_Min_2*** *are are assessed using currents only slightly above* ***Ilim_Min*** *to verify that the PSE will produce this transient level for Tlim_Min Per FIgure 33-15.*
PSE58	Short circuit power removal	33.2.7.7	SIFOS PSA	Begins within TLIM in Table 33–11. **Note**: ***Ilim*** *and* ***Tlim*** *within Table 33-11 do not have upper limits, and since port voltage is allowed to drop below* ***Vport_pse_min*** *per 33.2.7.7, there is effectively no lower limit to* ***Tlim*** *since PSE's may remove power with low voltage at any time according to 3.2.7.1.*	Test: pwrup_maxi **Tlim_1, Tlim_2** **Note**: ***Tlim*** *is only tested using Ilim_min to verify that* ***Tlim_min*** *is met and to verify that* ***Tcut_max*** *is met for the Type-2 PSE case.*
PSE59	Turn off time	33.2.7.8	SIFOS PSA	Applies to the discharge time from VPort_PSE to VOff with a test resistor of 320 kΩ attached to the PI.	Test: pwrdn_time **Toff**
PSE60	Turn off voltage	33.2.7.9	SIFOS PSA	Applies to the PI voltage in the IDLE state	Test: pwrdn_v **Voff**
PSE61	Current unbalance	33.2.7.11		Applies to the two conductors of a power pair over the current load range in accordance with Iunb in Table 33–11.	*Not Tested (See Sifos Technologies PhyView Analyzer, PVA-3000, for Coverage of PSE DC Unbalance Tolerance)*
PSE62	Type 2 PSEs in the presence of (Iunb / 2)	33.2.7.11		Meet the requirements of 25.4.4a	
PSE63	Power allocation	33.2.8		Not be based solely on historical data of power consumption of the attached PD. **Note**: *Power Allocation usually relates to a process spanning multiple powered PSE Ports. This specification generally defines the behaviors of a single PSE port.*	See Sifos Technologies **Multi-Port Test Suite**.
PSE64	PSE monitoring AC MPS component	33.2.9.1.1	SIFOS PSA	Meets "AC Signal parameters" and "PSE PI voltage during AC disconnect detection" parameters in Table 33–12	Test: mps_ac_vf **V_open**, **V_open_%Vport**, **Fp**, **AC_MPS_SR**, **Isac**
PSE65	PSE AC MPS component present	33.2.9.1.1	SIFOS PSA	When AC impedance at the PI is equal to or lower than |Zac1| in Table 33–12	Test: mps_ac_pwrdn **Tmpdo**, **I_hold_ac** *Implicitly covered by all pwrup_xxxx tests using PSA-3000 .*
PSE66	PSE AC MPS component absent	33.2.9.1.1	SIFOS PSA	When AC impedance at the PI equal to or greater than |Zac2| in Table 33–12	Test: mps_ac_pwrdn **Tmpdo** *Implicitly covered by all pwrup_xxxx tests using PSA-3000 .*
PSE67	Power removal	33.2.9.1.1	SIFOS PSA	When AC MPS has been absent for a time duration greater than TMPDO	Test: mps_ac_pwrdn **Tmpdo**
PSE68	PSE DC MPS component present	33.2.9.1.2	SIFOS PSA	IPort is greater than or equal to IHold min for at least TMPS min as specified in Table 33–11	Test: mps_dc_valid **Tmps**
PSE69	PSE DC MPS component absent	33.2.9.1.2	SIFOS PSA	IPort is less than or equal to IHold min as specified in Table 33–11	Test: mps_dc_pwrdn **I_hold**
PSE70	Power removal	33.2.9.1.2	SIFOS PSA	When DC MPS has been absent for a time duration greater than TMPDO	Test: mps_dc_pwrdn **Tmpdo**
PSE71	Not remove power	33.2.9.1.2	SIFOS PSA	When the DC current is greater than or equal to IHold max continuously for at least TMPS every TMPS + TMPDO	Test: mps_dc_valid **Duty_Cycle_tol**
DLL1	Reserved Fields	33.6	SIFOS PSA	Must parse and analyze TLV framing bytes from received PSE frame	Test: class_lldp **PSE_Source_Priority, PSE_MDI_Pwr_Sup**
DLL2	Data Link Layer classification standards compliance	33.6.1	SIFOS PSA	LLDP Frames from PSE comply with LLDP structural requirements 802.1AB	Test: class_lldp *Implicitly covered by all LLDP measurements and LLDP PD Emulations Utilized in this test and other Type-2 tests.*
DLL3	TLV frame definitions	33.6.1	SIFOS PSA	LLDP Frames from PSE comply with PoE TLV structural requirements of 802.3bc	Test: class_lldp *Implicitly covered by all LLDP measurements and LLDP PD Emulations Utilized in this test and other Type-2 tests.*
DLL4	Control State Diagrams	33.6.1	SIFOS PSA	Power Change Behaviors induced by PSE or PD follow state diagrams in clause 33.6.3	Test: class_lldp **PD_Power_Adjust_1, PSE_Adjust_Time_1, class_lldp_PD_Power_Adjust_2, PSE_Adjust_Time_2**
DLL5	Type 2 PSE LLDP PDU	33.6.2	SIFOS PSA	LLDP Framing transmitted within 10sec of POWER_ON state, or within 10.1 sec of actual power-up.	Test: class_lldp **PSE_LLDP_Time_2**
DLL6	Type 1 PSE LLDP PDU	33.6.2	SIFOS PSA	LLDP Framing transmitted when PSE activates LLDP subsystem.	Test: class_lldp **PSE_LLDP_Time_1** *(Soft limit relative to LAN Link since there is no visibility to PSE control variables.)*
DLL9	PSE Allocated Power Value Change	33.6.2	SIFOS PSA	LLDP PDU sent within 10 seconds that echo's PD's power request.	Test: class_lldp **PSE_Echo_Time_2, PSE_Echo_Time_2**
DLL10	PSE Power Control State Diagrams	33.6.3	SIFOS PSA	Operate according to state diagrams for power changes in 33.6.3	Test: class_lldp **PD_Power_Adjust_1, PSE_Adjust_Time_1, class_lldp_PD_Power_Adjust_2, PSE_Adjust_Time_2**

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